IN THE CLAIMS:

Amendments to the Claims

Please cancel claims 1-5 without prejudice or disclaimer of the subject matter thereof, and add the new claims in lieu thereof.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

6. (new) A semiconductor device comprising:

a memory which memorizes a first random number and other information; and

a memory address counter indicating an address of the memory,

wherein the first random number in the memory is set in the memory address counter and information in the memory is sent out non-contact condition with a time difference according to a numeric value of the first random number.

7. (new) An IC tag for transmitting first information to a reception unit, comprising:

a first memory which memorizes the first information;

a second memory which memorizes second information; and

a counter in which its count value indicates a bit address of the first memory,

wherein the IC tag carries out count-up or count-down of a count value of the counter according to a clock signal received from the reception unit and the IC tag sets information of the second memory as an initial value of the counter and after the count value of the counter reaches a specified code, the first information stored in the bit address of the first memory indicated by the count value is sent out to the reception unit successively.

8. (new) The IC tag according to claim 7,

wherein the second memories are provided in plural number and the IC tag sets the second information of any one of the second memories as an initial value of the counter.

9. (new) The IC tag according to claim 8, further comprising a mode switching portion,

wherein the IC tag selects the second information of any one of the second memories by means of the mode switching portion and sets it as an initial value of the counter.

10. (new) The IC tag according to claim 9,

wherein the mode switching portion is a flip-flop and the IC tag selects the second information of any one of the second memories according to a value of the flip-flop and sets it as an initial value of the counter.

11. (new) The IC tag according to claim 10,

wherein the specified code is zero.

12. (new) The IC tag according to claim 10,

wherein the counter and the second memory have the same bit number.

13. (new) The IC tag according to claim 10,

wherein the first information is comprised of at least identification number and an error detection code for detecting an error in the identification number.

14. (new) A reading method for reading the first information from an IC tag having a first memory which memorizes first information, a second memory which

memorizes second information and a counter in which a count value thereof indicates a bit address of the first memory to the reception unit, comprising:

transmitting a clock signal from the reception unit to the IC tag;

setting information of the second memory in the IC tag as an initial value of the counter;

performing count-up or count-down of a count value of the counter according to the clock signal; and

after the count value of the counter reaches a specified code, transmitting the first information stored in the bit address of the first memory indicated with the count value successively to the reception unit.

15. (new) The reading method according to claim 14,

wherein the second memories of the IC tag are provided in plural number and the second information of any one of the second memories is selected according to the mode switching signal and set up in the IC tag as an initial value of the counter.

16. (new) The IC tag according to claim 8,

wherein the specified code is zero.

17. (new) The IC tag according to claim 9,

wherein the specified code is zero.

18. (new) The IC tag according to claim 10,

wherein the specified code is zero.

19. (new) The IC tag according to claim 8,

*wherein the counter and the second memory have the same bit number.

20. (new) The IC tag according to claim 9,

wherein the counter and the second memory have the same bit number.

21. (new) The IC tag according to claim 10,

wherein the counter and the second memory have the same bit number.

22. (new) The IC tag according to claim 8,

wherein the first information is comprised of at least identification number and an error detection code for detecting an error in the identification number.

23. (new) The IC tag according to claim 9,

wherein the first information is comprised of at least identification number and an error detection code for detecting an error in the identification number.

24. (new) The IC tag according to claim 10,

wherein the first information is comprised of at least identification number and an error detection code for detecting an error in the identification number.